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A DIGITAL SYSTEM FOR SPEED AND PHASE CONTROL OF PHASED NEUTRON CHOPPER ARRAYS

by

E. BETTENDROFFER and J. EDER

1974



Joint Nuclear Research Centre
Ispra Establishment - Italy

Electronics Division

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Joint Nuclear Research Centre - Ispra Establishment (Italy)
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Luxembourg, May 1974 - 28 Pages - 11 Figures - B.Fr. 40,—

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All timing signals are derived from a central crystal clock which guarantees the required high longterm stability of speeds and phases. The settings may be adjusted manually or automatically by a computer through an appropriate interface (2).

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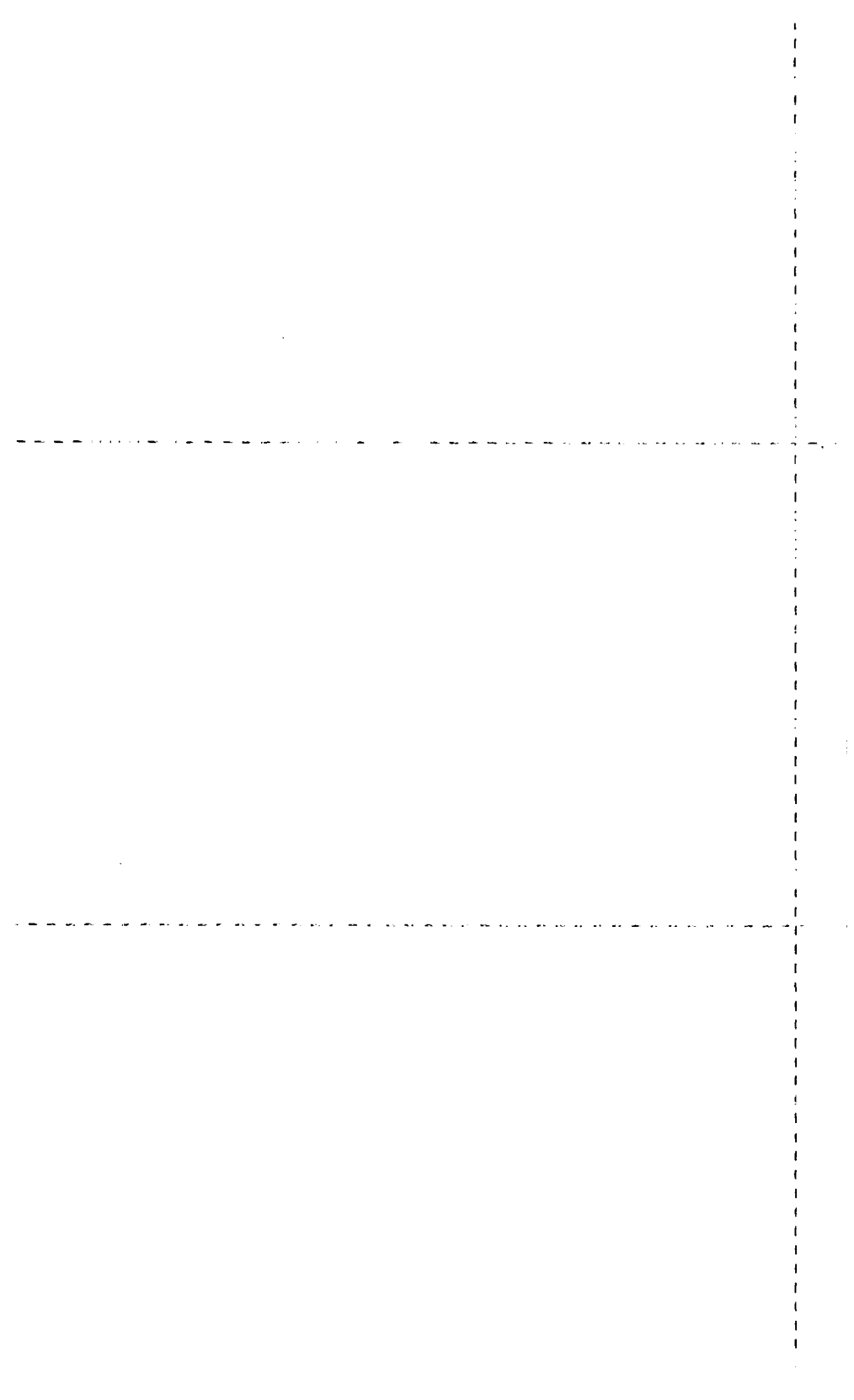
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ABSTRACT

Phased chopper arrays for slow neutron experiments require electrical drive systems with high stability in speed and phasing of the different rotors. In (1) a modular drive system is described which uses digital speed and phase control. This report gives the design of the control modules for speed and phase settings.

All timing signals are derived from a central crystal clock which guarantees the required high longterm stability of speeds and phases. The settings may be adjusted manually or automatically by a computer through an appropriate interface (2).

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1) PRINCIPLE OF OPERATION

Fig. 2 shows the control system for an array of 4 phased choppers. Each chopper has its own power drive module which contains also the control logic for motor start-up and positional feedback which forces the chopper to remain phaselocked with the timing signals F and $6F$.

A master generator provides the timing signals for the first chopper and determines the speed of the chopper array. It delivers also a pilot signal which serves as a general time base for all chopper control units. Phase angles between different rotors are always referred to this pilot. Delay generators produce by digitally delaying the pilot pulse frame the timing signals for the delayed choppers with the necessary frequency and phase relation.

With this arrangement the speed of all choppers can be changed or adjusted simultaneously, while the phase relations can be adjusted individually.

The timing signals F and $6F$ are pulse trains with pulse frequencies of one pulse resp. six pulses per chopper revolution. The period time T of the $6F$ signal is used for speed setting.

The relation between chopper speed and period T is given by :

$$\omega = \frac{1}{6 \cdot T} \cdot 60 = 10^7 \cdot \frac{1}{T} (\mu\text{s}) \text{ rpm} \quad (1)$$

T can be chosen between

$$9999 \mu\text{s} \hat{=} 1000 \text{ rpm}$$

and

$$400 \mu\text{s} \hat{=} 25000 \text{ rpm}$$

in steps of 1 μs . This corresponds to a resolution of 0.5 % at 25000 rpm resp. 0.02 % at 1000 rpm.

The speed stability however depends only on the crystal clock and is in the order of $5 \cdot 10^{-4}$.

In a similar manner instead of phase angles the delay time D between the aperture times of a chopper referred to the master chopper is used as set value for the delay generators due to

$$\varphi = 360 \cdot \frac{\omega}{60} \cdot D = 60 \cdot 10^{-6} \cdot \omega \cdot D (\mu\text{s}) \text{ } ^\circ \quad (2)$$

Since the delay can be adjusted in steps of 1 μs too, the angular resolution is

$$0.06^\circ = 3.6' \text{ at } 1000 \text{ rpm}$$

and

$$1.5^\circ \text{ at } 25000 \text{ rpm}$$

Manual or automatic (via computer interface) input of the set values for speed and delay can be chosen.

Since the chopper-drives are phaselocked to the timing signals F and $6F$, any step change of the signal frequency must be avoided if we want to keep all choppers in synchronism. Therefore a special circuit is built in, which smoothes the steps provoked by an arbitrary change of a set value in a way, the phase lock system can follow without losing synchronism.

For safety reasons the maximum speed must be limited to ≤ 25000 rpm. This corresponds to a period set value of $\geq 400 \mu s$. If by error a period value below this limit is selected (manually or automatically), the frequency of the timing signals is automatically limited.

2) MASTER GENERATOR (Fig. 4)

2.1. Manual-mode

When supply voltage is applied, the one-shots I and II are triggered by "RC" (fig. 5). One-shot I causes the pre-selected number (3000 for example) to be stored in the latches (fig. 6). One-shot II produces a parallel load of the up/down counters, which means that the value 3000 is fed to the counter outputs through the data input line. Since the data inputs of the 0.1 μ s decade (fig. 7) are at logical 0, this counter is loaded with zero. Thus, in reality, the loaded value is not 3000 but 30000. The A and B inputs of the upper comparators both "see" the number 30000, their outputs $A > B$ and $A < B$ are at logical zero, and the output pulses of the slew generator (fig. 5) are inhibited.

The 400 μ s interlock is controlled by the 400 μ s coincidence : When the contents of the up/down counters become smaller than 400 μ s, the outputs of the interlock (representing decades 1, 2 and 3) remain at 400 (fig. 6). In our example ($P = 3000 \mu$ s) the value 000 is fed through the interlock and the A inputs of the lower comparators are 30000. When the synchronous decade counter (fig. 7), supplied by the 10 Mhz crystal oscillator, reaches 30000, the $A > B$ outputs and consequently the output of the Or-gate (fig. 8) become zero. With this edge the decade counter is reset (and recommences to count) and one-shot III is triggered.

This one-shot gives the 6F output signal (after level translation) and the clock pulses for the divide by six counter, which will deliver an output pulse at each sixth 6F pulse. This pulse (after level translation) is used as 1 F output signal and also resets the divide by six counter to zero.

Assume the value 4000 is now read into the latches by pressing the load pushbutton. Now, the $A > B$ output of the upper comparators becomes "1" and the slew generator pulses are fed to the up input of the up/down counters until they have reached 40000.

After the first slew generator pulse, the up/down counter outputs and also the A inputs of the lower comparators are 30001. Thus, the decade counter will count up to 30001 before the lower comparators deliver an output signal. In this way the period of the 6F output signal follows the up/down counter step by step, increasing by steps of $0.1 \mu\text{s}$ at a rate depending on the slew generator frequency. The decreasing mechanism is similar.

The slew generator operates as follows : The oscillator is an unijunction transistor with recurrence frequency depending on the RC value. The fourth decade and the three last bits of the third decade of the up/down counters are used to produce a coincidence at 4 different period values. Each coincidence

commutates to ground a capacitor at predetermined period values, thus increasing or decreasing the total capacitor value and reciprocal the slew rate.

<u>Period value</u>	<u>Slew rate</u>
9999 μ s \geq P \geq 4000 μ s	30 ms
4000 " > P \geq 2000 "	70 ms
2000 " > P \geq 1000 "	200 ms
1000 " > P \geq 600 "	300 ms
600 " \geq P \geq 400 "	600 ms

2.2. Automatic-mode

The period value to be stored into the latches is supplied by a computer, which also delivers the load signal. After the value has been inscribed, the generator delivers an acknowledge pulse to the computer. See also [2] .

2.3. Specifications

The Master Generator is housed in a two-units ESONE plug-in (see fig. 1). A second plug-in contains the common power supply for one Master Generator and up to three Delay Generators.

Note : The generators and their power supply should be operated only in the supplied chassis.

Since the standard ESONE wiring has been modified at the present device, it would also be dangerous to operate it in the chassis instruments which are designed in the ESONE standard.

Don't exchange the position of the power supply with a generator and vice versa. However, the positions of the generators may be chosen arbitrarily.

- 6 F output signal : period P_1 variable between 400 and 9999 μs ,
by steps of 0.1 μs .
- 1 F output signal : period $P_2 = 6P_1$, synchronous with 6F
(fig. 3). Variation : 2400 to 59994 μs
by steps of 0.6 μs .

Common characteristics of both output signals :

- pulse width : 2 $\mu\text{s} \pm 10 \%$
- quiescent level : + 15 V
- pulses negative from + 15 V to ground
- capability of driving up to 10 MHTL
circuits ($I_{\text{sink}} = 30 \text{ mA}$) from each output
connector, including the test outputs.

- slew rate : ≈ 30 ms to ≈ 600 ms in 5 ranges. Automatic range commutation at predetermined values of P1. The rate value can be adjusted by a factor 1 : 3 by front panel potentiometer.

Readout : - instantaneous value of P1 (four decades) displayed by seven segment indicators.

Clock frequency : 10 Mhz, produced by a crystal oscillator

Operating modes : - Manual : presetting and loading of the desired period value are executed by the operator.

- Automatic : the functions are computer controlled.

Power supply : + 5 V, 10 A (N.V. Delta Elektronika Type M5-10)
+ 15 V, 150 mA.

3) DELAY GENERATOR (Fig. 9)

3.1. Manual-mode

For the operation of the decade command card (fig. 6) and the command card (fig. 5) refer to 2.1. of the Master Generator.

The 1F pulse issued from the Master Generator starts the delay counter (fig. 10), supplied by the 1 μ s clock pulses from Master Generator. When the counter reaches the presetted delay value, the output pulse of the comparator simultaneously :

- 1) resets the delay counter and inhibits the clock pulses
- 2) resets the D > 6P interlock
- 3) triggers the 1F' output one-shot.

The D > 6P interlock operates as follows : When the second 1F pulse comes in before the comparator delivers an output pulse (that means : when the presetted delay value > 1F period), this 1F pulse is fed through the interlock and takes over the 3 functions described above ; during this time, the comparator pulse is inhibited. When the delay value becomes $\leq 6P1$, the comparator pulse passes, while the 1F pulse is inhibited.

When D = 0, the output of the comparator is permanently logical "1" and the 1F pulse is used as output signal.

1F' resets a divide by six counter, the outputs of which control the select inputs of a multiplexer (fig. 11).

The same signal, slightly delayed is applied to the corresponding data input of the multiplexer and appears at its output and triggers the one-shot. The latter delivers the output signal $6F'$, the trailing edge of which is used to advance the divide by six counter by one position, enabling one of the five paralleled data inputs of the multiplexer.

The multiplexer output signal also resets a decade counter, which is supplied with the clock pulse issued from PC20224 (Master Generator). The contents of this decade counter are compared with the value of P1 (Master Generator) ; when this value is reached, the comparator output signal is applied to one of the 5 paralleled inputs of the multiplexer. This process is repeated five times. The fifth output pulse sets the divide by six counter to a position corresponding to zero, so enabling the $1F'$ signal. In this way, each $1F'$ pulse is used as reference to the $6F'$ pulses, thus adjusting $6F'$ to the instantaneous delay value.

3.2. Automatic-mode

The delay value and the "load" pulse are supplied by the computer (same procedure as with Master Generator, see 2.2.).

3.3. Specifications

Like the Master, the Delay Generator is housed in a two units ESONE plug-in (see fig. 1).

Output signal 1F' : - period equal to P2 of Master Generator
- delay (with respect to 1F of Master Generator) :
variable between 0 and the instantaneous value of P2, up to a maximum of 9999 μ s), by steps of 1 μ s (fig. 3).
- instantaneous delay value displayed by 7 segment indicators.

Output signal 6F' : - period equal to P1 of Master Generator,
synchronous with 1F'.

Common characteristics of both output signals :

- pulse width : 2 μ s \pm 10 %
- quiescent level : + 15 V
- pulses negative from + 15 V to ground
- capability of driving up to 10 MHTL circuits (I sink = 30 mA) from each output connector, including the test outputs
- slew rate : adjustable between 0.5 s and 1.5 s by front panel potentiometer

- Clock frequency : - 1 Mhz, supplied by Master Generator
- Operating modes : - Manual : presetting and loading of the
delay value by operator
- Automatic : the functions are computer
controlled.

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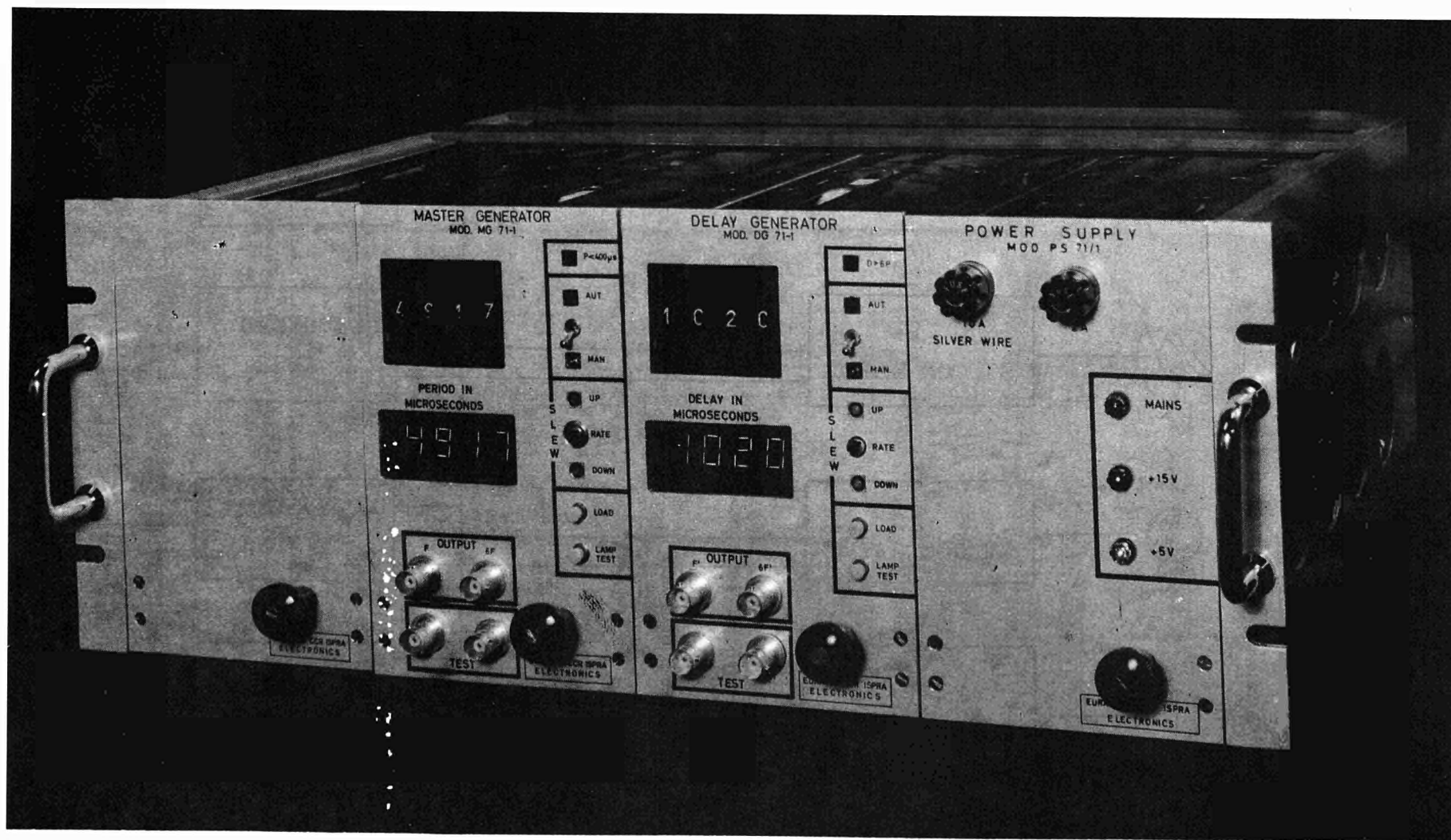


FIG. 1

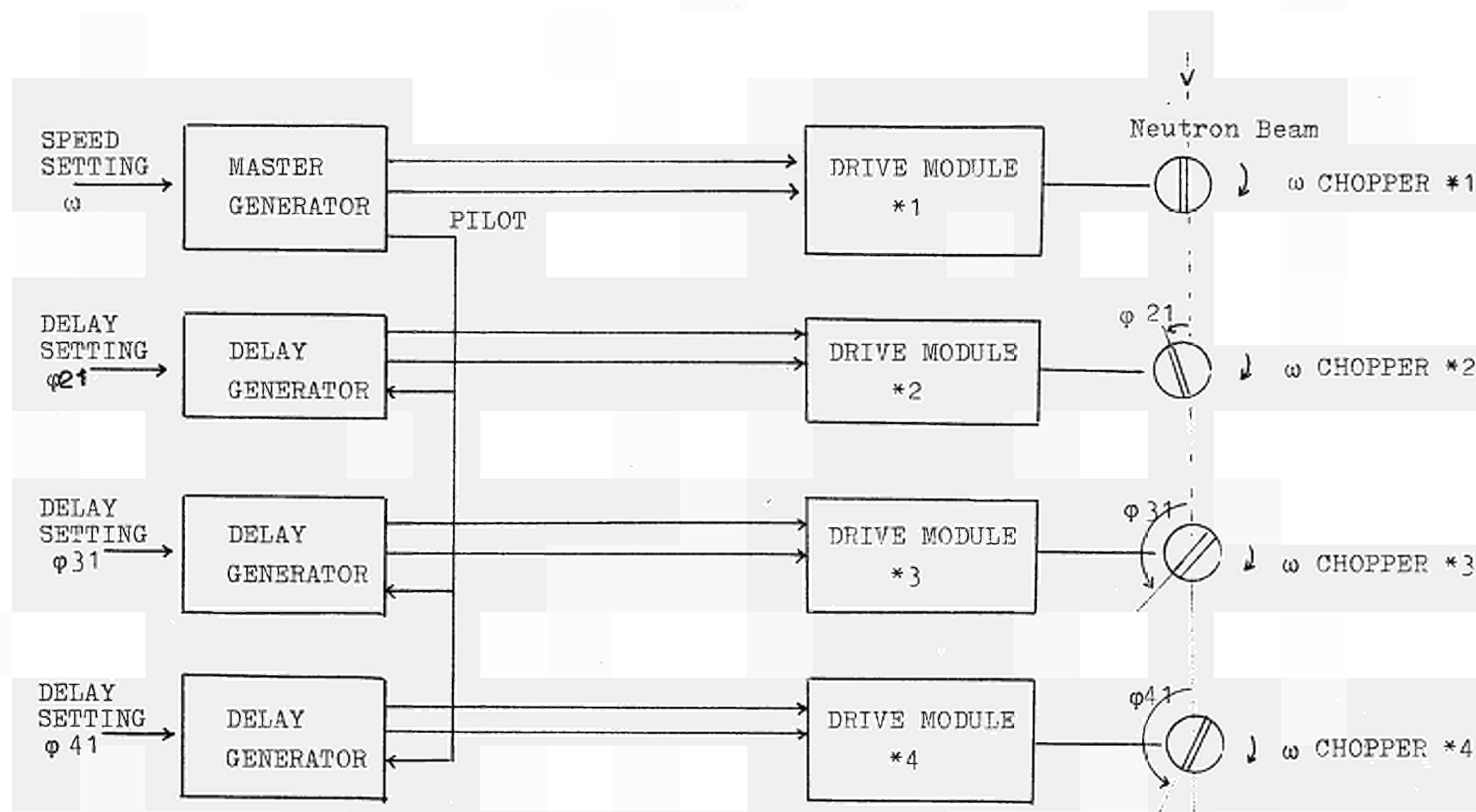
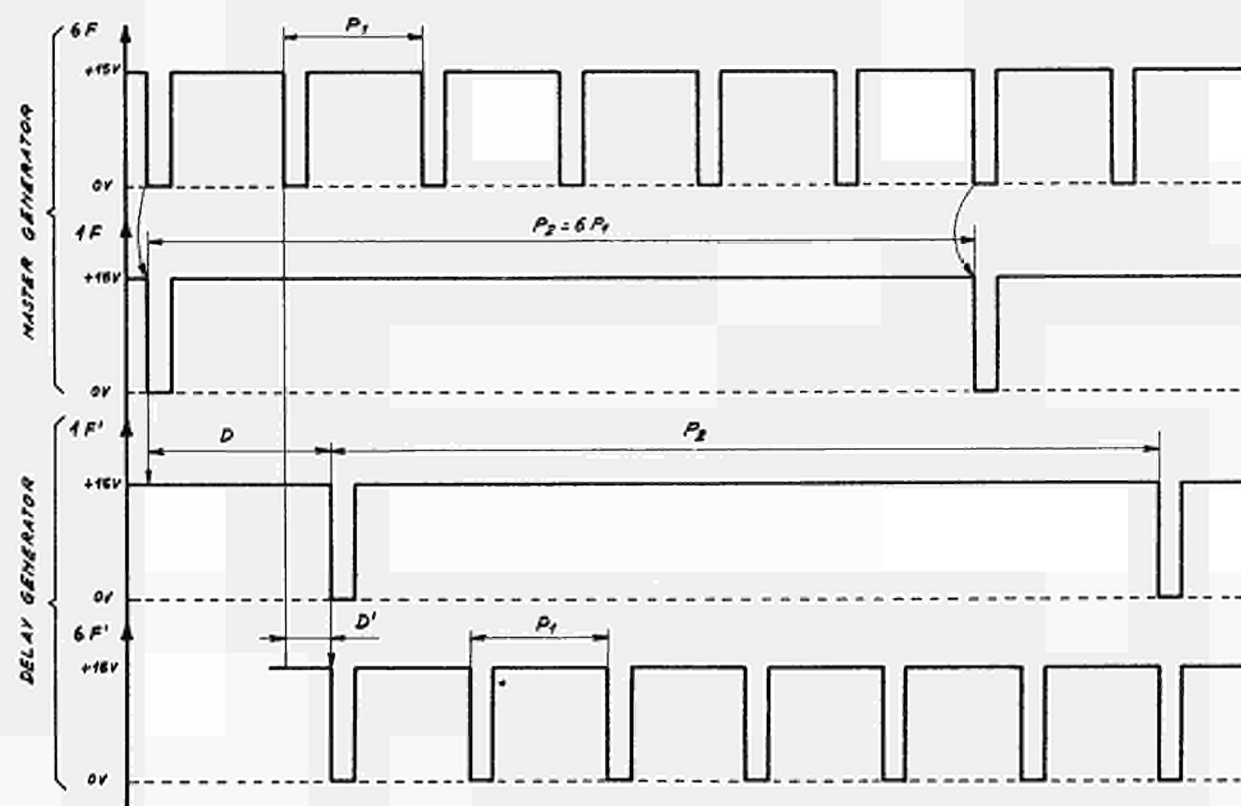
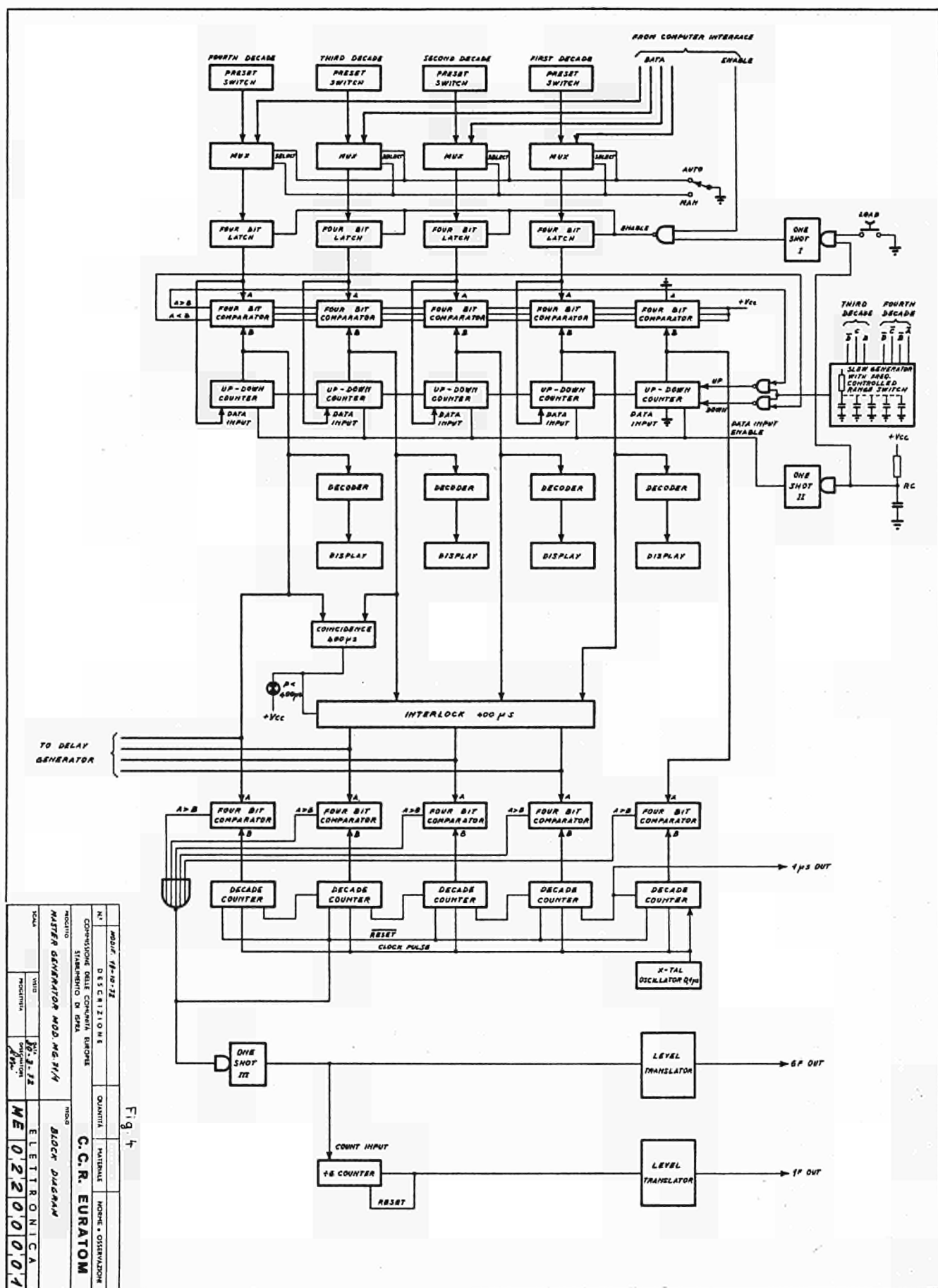


Fig. 2 CONTROL OF 4 PHASED CHOPPERS



MOD. 18-10-72			
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COMMISSIONE DELLE COMUNITÀ EUROPEE STABILIMENTO DI ISPRA			
C.C.R. EURATOM			
PROGETTO	TITOLO		
DELAY GENERATOR MOD. DG 2	TIMING DIAGRAM		
SCALA	VISTO	DATA	ELETTRONICA
	PROGETTISTA	30-3-72	
	DISEGNATORE	Rm.	
ME 02100007			



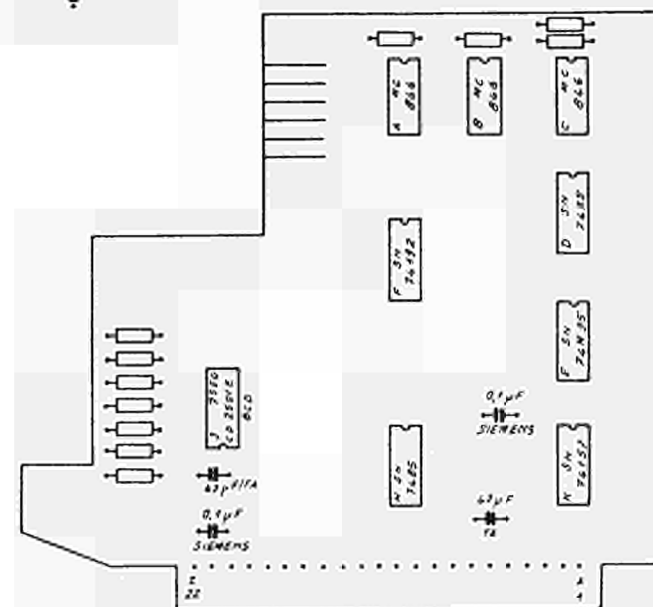
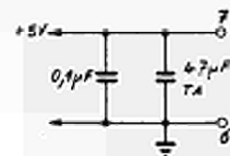
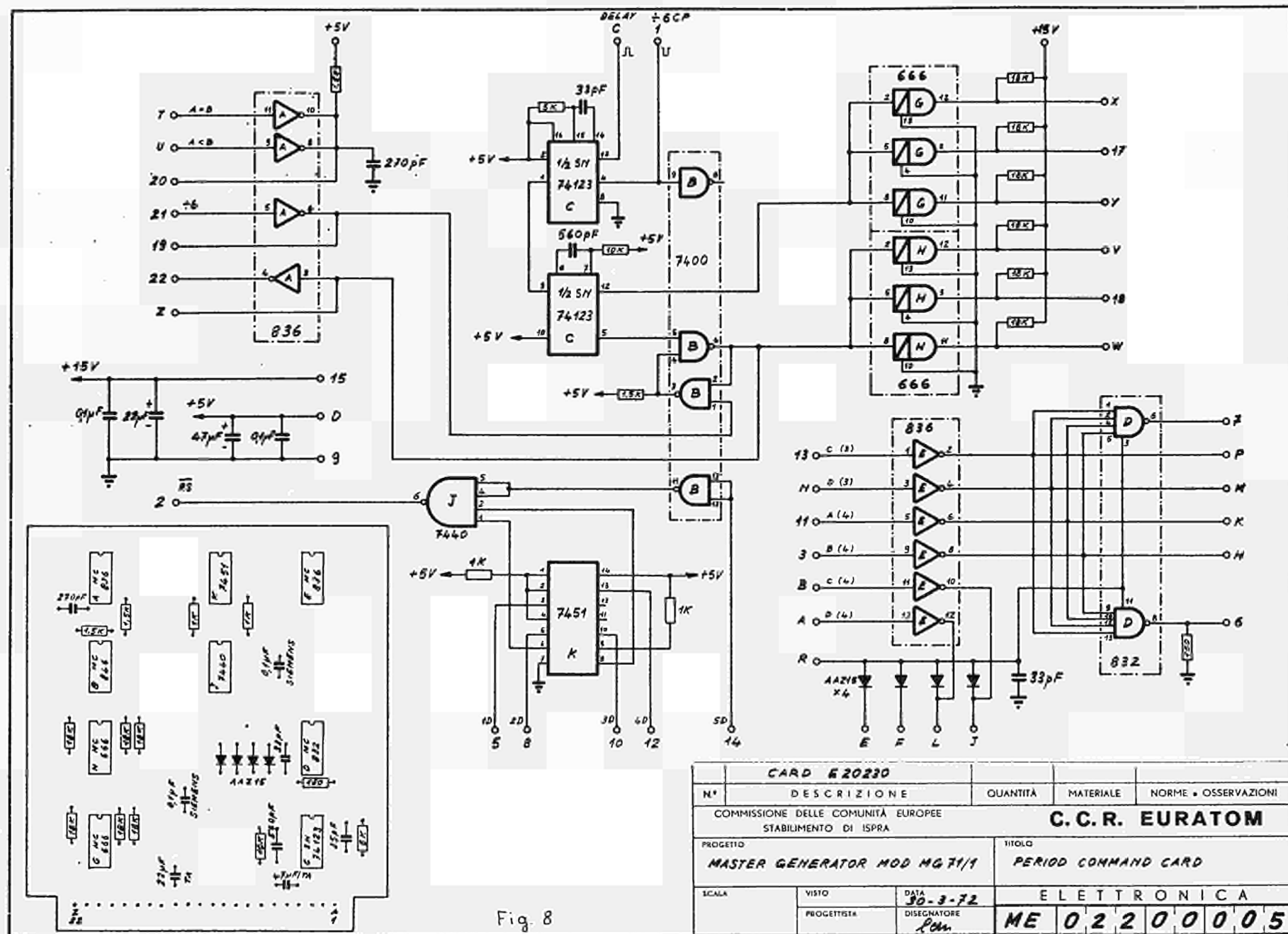
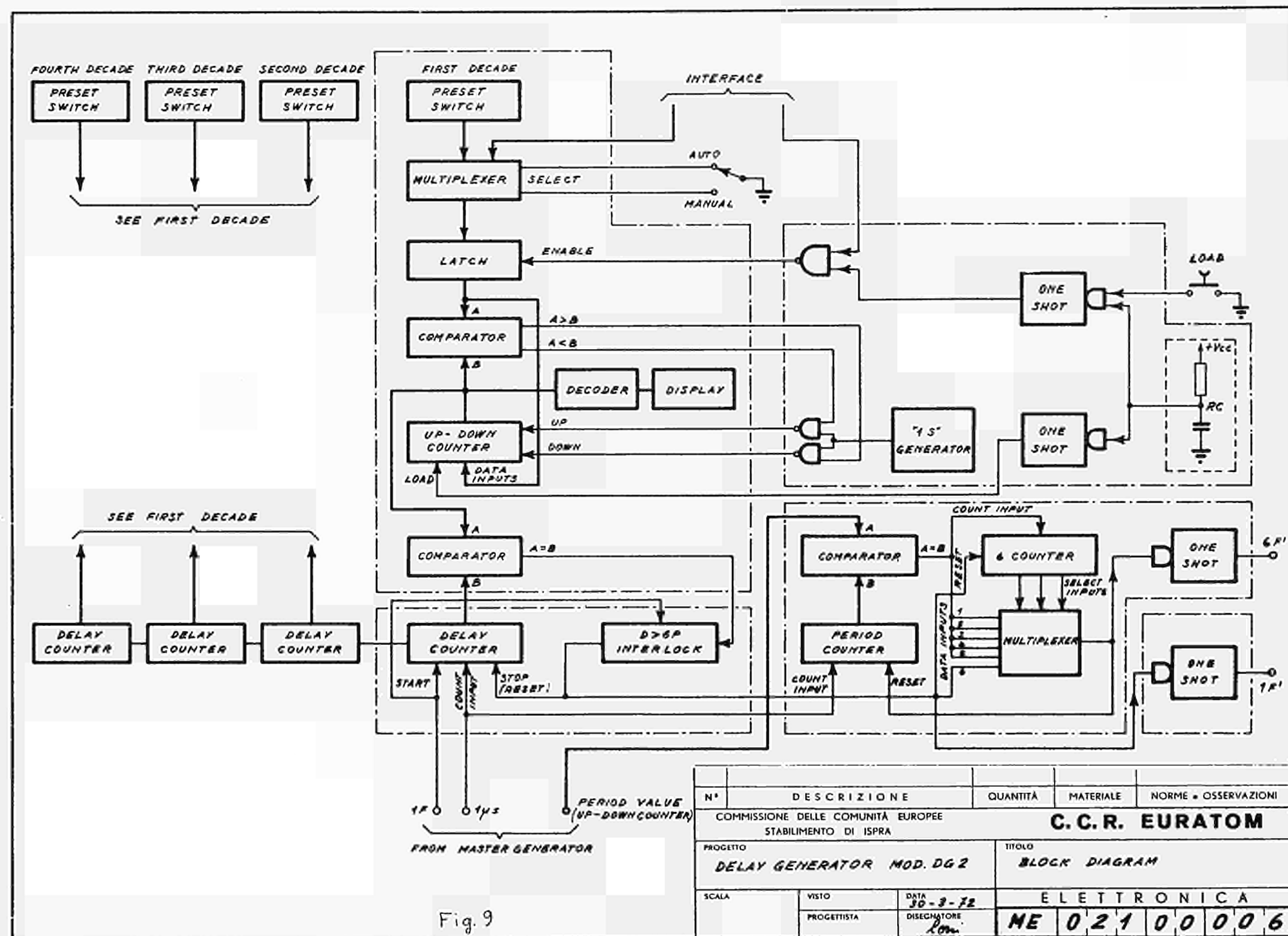
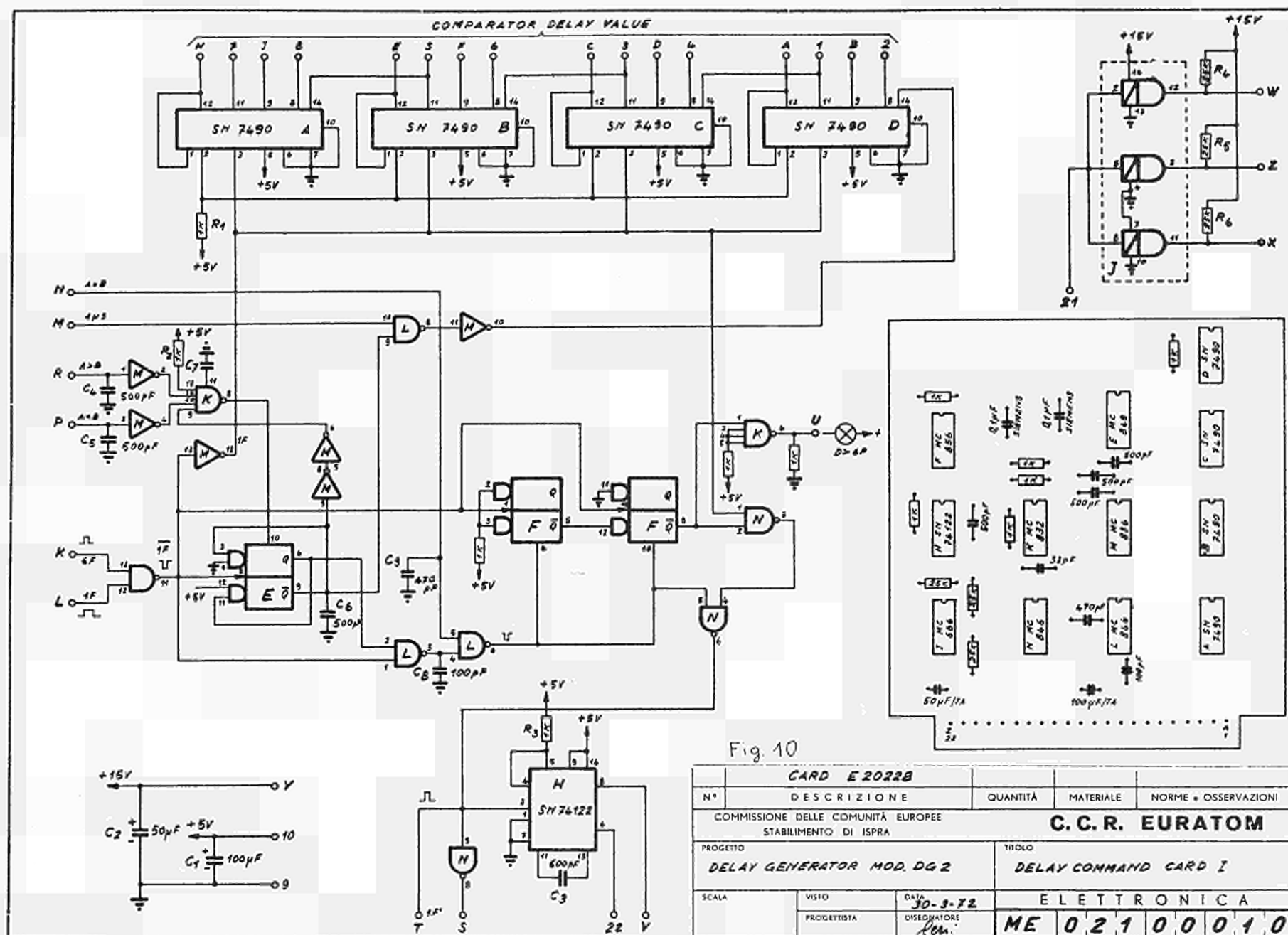


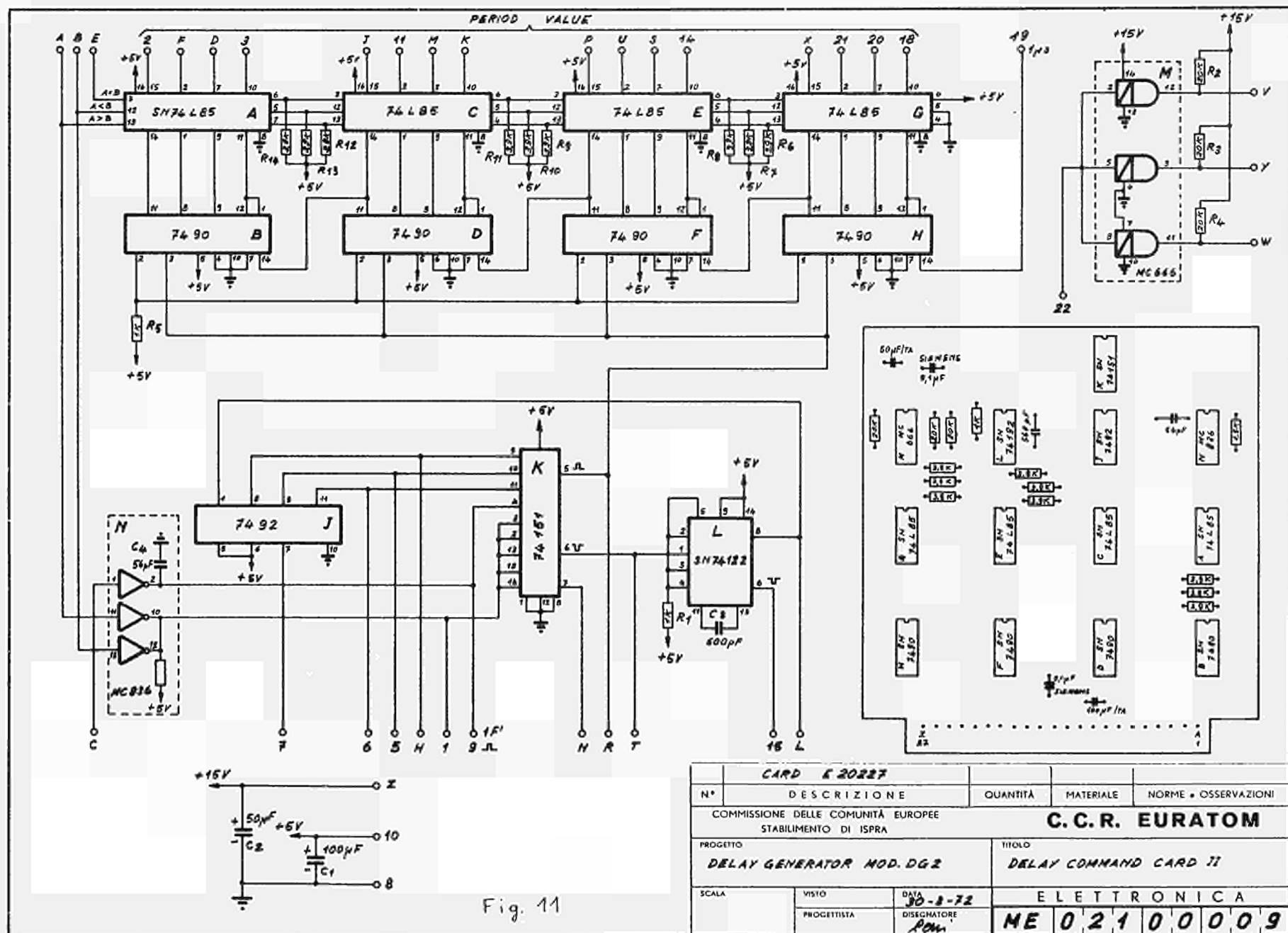
Fig. 6

CARD E20225					
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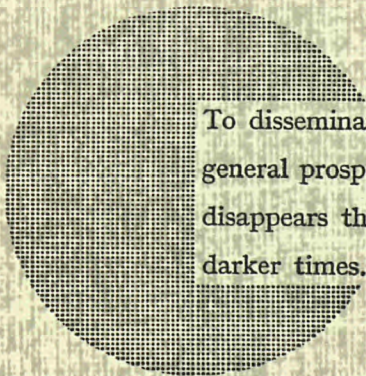




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To disseminate knowledge is to disseminate prosperity — I mean general prosperity and not individual riches — and with prosperity disappears the greater part of the evil which is our heritage from darker times.

Alfred Nobel

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